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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 04/12/2005

Hewlett Packard Company
Intellectual Property Administration
P O Box 272400
Fort Collins, CO 80528-9599

EXAMINER	
SAFAIPOUR, HOUSHANG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 04/12/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/626,625	07/27/2000	Robert G. Gann	10001227-1	1161

TITLE OF INVENTION: METHOD AND SYSTEM FOR CALIBRATING A LOOK-DOWN LINEAR ARRAY SCANNER UTILIZING A FOLDED OPTICAL PATH

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$1400	07/12/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 12/04) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 04/12/2005

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/626,625	07/27/2000	Robert G. Gann	10001227-1	1161

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APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$1400	07/12/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
SAFAIPOUR, HOUSHANG	2622	358-474000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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7590 04/12/2005

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EXAMINER	
SAFAIPOUR, HOUSHANG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 04/12/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 632 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 632 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 12/04) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	09/626,625	GANN, ROBERT G.	
	Examiner	Art Unit	
	Houshang Safaipour	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Appeal Brief filed on 2/7/05*.

2. ☒ The allowed claim(s) is/are *1,3-11 and 13-29*.

3. ☒ The drawings filed on *27 July 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EDWARD COLES
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

Applicant's arguments filed, via Appeal Brief, on February 7, 2005 are persuasive. Rejection of claims 1, 3, 4, 6, 7, 8, 10, 11, 13-22, 24, 26, 27 and objection to claims 23 and 25 have been withdrawn accordingly.

Reasons for Allowance

Claims 1, 3-11 and 13-29 are allowed.

This is examiner's statement of reasons for allowance.

The instant invention recites a method of calibrating a look-down digital imaging device comprising:

focusing on a calibration area within the look-down digital imaging device;

scanning the calibration area within said look-down digital imaging device to capture image data for said calibration area;

analyzing said captured image data for said calibration area; and

adjusting the imaging of said look-down digital imaging device based on said analysis of said captured image data for said calibration area.

The features identified, in combination with other claim limitations, are neither suggested nor discussed by the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Houshang Safaipour whose telephone number is (571)272-7412. The examiner can normally be reached on Mon.-Thurs. from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L Coles, Sr. can be reached on (571)272-7402. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Houshang Safaipour
Patent Examiner
Art Unit 2622
April 1, 2005

EDWARD COLES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

PATENT APPLICATION
Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
10001227-1	09/626,625
APPLICANT	
Robert G. Gann	
FILING DATE	**GROUP**
July 27, 2000	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
HS	1A	5,227,896	July 13, 1993	Ozaqa et al	358	474
HS	1B	5,515,181	May 7, 1996	Iyoda et al	358	474
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Canon Visual Communication Systems Document # 4150 dated December 1998
	1R	
	1S	

EXAMINER	DATE CONSIDERED
HS	8/5/03

Rev 05/00 (PTO-1449)

PATENT APPLICATION
Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
10001227-1	09/626,625	1161

APPLICANT	
Robert G. Gann	
FILING DATE	GROUP
July 27, 2000	2622

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
HD	1A	4,967,233	10/30/1990	Buchar et al.	
↓	1B	5,969,845	10/19/1999	Tsai et al.	
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
HD	1L	WO98/44718A2	10/08/1998	AGRIS-SCHOEN VISION		
↓	1M	WO98/44718A3	10/08/1998	AGRIS-SCHOEN VISION		
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Foreign Seach Report dated Dec. 19, 2003, 3 pages
	1R	
	1S	

EXAMINER	DATE CONSIDERED
[signature]	7/11/07

Rev 10/03 (PTO1449)

Notice of References Cited	Application/Control No. 09/626,625	Applicant(s)/Patent Under Reexamination GANN, ROBERT G.	
	Examiner Houshang Safaipour	Art Unit 2622	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,721,465	04-2004	Nakashima et al.	382/318
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application No.	Applicant(s)	
	09/626,625	GANN, ROBERT G.	
	Examiner	Art Unit	
	Houshang Safaipour	2622	

ISSUE CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS		CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)						
358	474		358	406	504					
INTERNATIONAL CLASSIFICATION			250	234	234					
H04N	1104		348	79	95	180	150			
H04N	1100									
H04N	1146									
H01J	31/14									
H04N	17/00									

(Assistant Examiner) (Date)

K Davis 4-7
(Legal Instruments Examiner) (Date)

EDWARD COLES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY
(Primary Examiner) (Date)

Total Claims Allowed: 27

O.G. Print Claim(s)	O.G. Print Fig.
1	1

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	[illegible]	31		61		91		121		151		181
X	2		32		62		92		122		152		182
2	3		33		63		93		123		153		183
3	4		34		64		94		124		154		184
4	5		35		65		95		125		155		185
5	6		36		66		96		126		156		186
6	7		37		67		97		127		157		187
7	8		38		68		98		128		158		188
8	9		39		69		99		129		159		189
9	10		40		70		100		130		160		190
10	11		41		71		101		131		161		191
X	12		42		72		102		132		162		192
11	13		43		73		103		133		163		193
12	14		44		74		104		134		164		194
13	15		45		75		105		135		165		195
14	16		46		76		106		136		166		196
15	17		47		77		107		137		167		197
16	18		48		78		108		138		168		198
17	19		49		79		109		139		169		199
18	20		50		80		110		140		170		200
19	21		51		81		111		141		171		201
20	22		52		82		112		142		172		202
21	23		53		83		113		143		173		203
22	24		54		84		114		144		174		204
23	25		55		85		115		145		175		205
24	26		56		86		116		146		176		206
25	27		57		87		117		147		177		207
26	28		58		88		118		148		178		208
27	29		59		89		119		149		179		209
[illegible]	30		60		90		120		150		180		210

Search Notes

Application No.	Applicant(s)	
09/626,625	GANN, ROBERT G.	
Examiner	**Art Unit**	
Houshang Safaipour	2622	

SEARCHED			
Class	Subclass	Date	Examiner
358	474	7/17/07	HS
↓	406		
↓	504		
250	234		
↓	236		
348	79		
	95		
	180		
	190		
	187		
	188		
↓	189		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
358	474 406	8/7/07	HS
↓ 250	504 234		
348	79 95		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
East	3/3/05	HS
Consulted w/ Ed Colen Fan Lee	↓	↓

pulses are generated thereby in response to a system data clock which effectively generates 1,700 clock pulses. The Clock 1 pulses are timed to occur during the presence of the 850 odd bits of data present in the 1,700 bit data stream supplied to the Data In input 50. In this way, alternate bits of data present in the data stream applied to conductor 50 which correspond to the 850 odd data bits therein are serially clocked into the shift register 44 so that upon the expiration of 850 clock pulses the shift register 44 will be loaded with the 850 odd bits of data within the data stream. Conversely, in identical structure employed for the column conductors present in row 36 in Figure 2, a Clock 2 input also generated in Figure 6 is utilized. The Clock 2 input as shall be seen below generates 850 synchronously timed clock pulses which correspond to the presence of the 850 even bits of data presentin the 1,700 bit data stream supplied to the Data In input of the 850 bit shift register employed for the evenly designated connector pads in row 36. Using this approach, it will be appreciated that the data need not be separated for the application to the odd and even column connector pads in rows 34 and 36 in Figure 2 and similarly separate connection from a 1,700 bit driver arrangement is not necessary.

The Clear input to the shift register 44 which is connected to conductor 56 is employed to clear the shift register 44 each time 850 bits of odd column information have been written into the shift register 44 and subsequently loaded in parallel into the 850 latches 46. Thereafter, while the latches 46 are being read, new column information may be clocked into the 850 bit shift register 44 so that information may be written into the shift register 44 and read from the latches 46 in a flip flopped or alternating manner well-known to those of ordinary skill in the art. The Set input to the 850 bit shift register 44 connected on conductor 48 is not generally employed except, for the purpose of writing an initializing 1 into stage one of the first shift register in the 850 bit shift register 44 or for diagnostic purposes which are not here relevant.

The output of the 850 bit shift register 44 is applied in parallel though conductors 60_1-60_{850} to the individual latches within the 850 latch array 46. The operation of the shift register 44, as will be readily appreciated by those of ordinary skill in the art, is that the same is cleared subsequent to the gating of information therefrom into the 850 latch array 46. This is done by the application of a clear pulse to a conductor 56. Once clearing has occurred a 1 may be written into the initial stage thereof by the application of a 1 level to the set input thereof and thereafter data and clock signals on conductors 50 and 54 are awaited. More particularly, serial data is applied to conductor 50 in the manner aforesaid so that a serial stream of 1,700 bits is applied thereto. As the data is applied Clock 1 pulses are applied to conductor 54 in such a manner that 850 clock pulses timed to occur during the presence of the odd data pulses within the data stream are applied to conductor 54. This will cause, in a manner well-known to those of ordinary skill in the art, the odd data pulses present in the serial data stream applied to conductor 50 to be clocked through the 850 bit storage locations within the shift register 44 in a serial manner.

Once 850 clock pulses have been supplied to the conductor 54, the clock pulses are terminated in a manner which will be described in greater detail in connection with Figure 6. Since 850 bits of data corresponding to the 850 odd bits of data within the data stream are now located into the shift register 55 the same are now present at the outputs thereof on conductors 60_1-60_{850}. Once this occurs a latch pulse is applied in parallel to each of the 850 latches within the latch array 46. Upon this occurence of the latch pulse which is applied to conductor 62 in the manner indicated in Figure 5, the 850 bits of data present on conductor 60_1-60_{850} are latched into the latch array 46. Thereafter, the shift register 44 may be cleared to await a next group of 850 bits of information associated with the next 1,700 bits of data for the row within the display. It will also be appreciated that what has just been described for the odd column driver array shown in Figure 5 will also be occuring with respect to the even column driver array, not shown, under the auspices of the Clock 2 clocking signal.

The latch array 46 may comprise 850 individual latches or alternatively a plurality of multi-latch chips may be employed. In either case the latch input to each chip is connected in parallel to conductor 62. Each of the latches act in the manner well-known to those of ordinary skill in the art to load any data supplied to the inputs thereto on conductors 60_1-60_{850} during the presence of a latching pulse on conductor 62. Once a bit is latched into an individual latch within the array 46, it is present on the outputs of the individual latches here indicated as connected to conductor 64_1-64_{850} until new data is latched into the latches by the application a new enable level on conductor 62. This structure would also be present in the drive circuit for the even columns.

Once the data from the shift register has been latched into the latch array 46 it is available on conductors 64_1-64_{850} and as indicated in Figure 5 is applied to one input of the plurality of AND gates 48_1-48_{850} it being appreciated that one AND gate is assigned to each latch within the latch array 46. At this time, as aforesaid, a new write operation may be initiated for the 850 bit shift register 44 as well as that in the even column array. A second

input to each of the AND gates 48_1-48_{850} is connected to the conductor 66. The conductor 66 is connected to an output annotated Strobe which is a system generated pulse which occurs subsequent to the latching level applied to conductor 62. The strobe level it will be appreciated is employed to strobe the contents of each latch stage within the latch array 46 through the AND gates 48_1-48_{850} to the outputs thereof herein annotated C_1, C_3, C_5 and C_{1699}.

Thus, each of AND gates 48_1-48_{850} acts in a manner well-known to those of ordinary skill in the art to produce a high at the outputs thereof only when both of the inputs thereto are high and only for the duration of such high inputs. Therefore, it will be appreciated that when a high level is applied to the strobe conductor 66 whatever input is supplied to the AND gates 48_1-48_{850} on conductors 64_1-64_{850} is applied to the outputs of the AND gates and for the duration of the strobe pulse. The outputs of each of the AND gates 48_1-48_{850} as indicated by the terminal annotations C_1-C_{1699} are connected to the odd column connector pads disposed within the row of connector pads 34 illustrated in Figure 2.

Conversely, a corresponding circuit to that shown in Figure 5 employing a Clock $_2$ input for the shift register 44 would be connected in a corresponding manner to the even column connector pads located in the row of connector pads 36 on the frame illustrated in Figure 3. This circuit would have it's corresponding AND gates strobed at the same time as AND gates 48_1-48_{850}. Thus both the odd and even column lines will be written with appropriate 1's and 0's at the same time. As the entire circuit illustrated in Figure 4 can be implemented in CMOS, it will be appreciated that the circuits and the connections therefrom may be mounted entirely within the structure of the frame illustrated in Figure 3, in precisely the manner described in U.S. Patent Application Serial No. 728,602 as aforesaid. Thus, in the manner described in Figure 5, 850 bits of column information assigned to a particular row on the display will be clocked into the shift register 44, latched within the latch array 46 and thereafter strobed to the column connector pads in the row of column connector pads 34 shown in Figure 2. This also occurs at the same time for the even column connector pads in row 36. Once this is done, the predetermined row on the display to which this data is assigned is strobed by having a zero level applied thereto so that data on each of the column conductors is written into the display by virtue of the electrophoretic particle propagation which occurs as a result of the selective energizing of each intersection within that row. This procedure is continued until all 1,700 column positions for each of the 2,200 rows had been written. Once this is achieved no further writing takes place until what is displayed is to be changed since, as aforesaid, the display exhibits hysteresis.

While a technique for supplying a 0 volt level to each of the odd and even row connector pads present in columns 38 and 40 in Figure 2 has not been described herein, those of ordinary skill in the art will readily appreciate that the same may readily be achieved through a simple modification of a driver circuitry illustrated in Figure 5 or, alternatively, other simplified driving arrangements could be employed. Thus, identical structure to that employed for the odd and even columns, as shown in Figure 5, could be employed for each of the odd and even connector pads in columns 38 and 40 except that 1,100 bit shift registers and latch arrangements would be configured. Here each of the 1,100 bit shift registers would be initialized so that a 1 is present in each stage thereof and a 0 is then written into the first stage of each 1,100 bit register. Each 1,100 bit shift register may be clocked in an alternate manner each time the column driver arrangement for the odd and even columns as shown in Figure 5 in enabled or strobed and the 1,100 bit latches thereof are strobed in an alternate manner when the 1,700 bit column latches are strobed. A row is written when a 0 volt level is applied to a row conductor 4 and 1 and 0 information is present on all 1,700 column lines 10.

Referring now to Figure 6 there is shown a block diagram schematically illustrating an exemplary embodiment of a circuit suitable for separating data between odd and even columns. The circuit illustrated in Figure 6 serves to generate the $Clock_1$ input described in connection with Figure 5 as well as a $Clock_2$ input which would be employed in a circuit identical to that illustration in Figure 5 to drive even columns C2, C4, C6 . . . C1700. The use of separate odd and even driver circuits such as illustrated in Figure 5 is preferred in order to permit installation of such driver circuits in association with the odd and even column connection pads illustrated in Figure 2. Those of ordinary skill in the art will appreciate that the circuit of Figure 5 may be replaced by a 1700 bit arrangement and under these circumstances direct connection to odd and even connection pads could be implemented. This of course would avoid the need for the use of the exemplary embodiment of a circuit for separating data between odd and even columns as illustrated in Figure 6

The function of the exemplary circuit illustrated in Figure 6 is to separate a stream of data clock pulses into two streams of clock pulses herein designated $Clock_1$ and $Clock_2$ which represent the odd and even clock pulses respectively within the stream of data clock pulses. Data clock pulses as

shall be seen in greater detail below are pulses which are synchronized to the system clock and correspond in width thereto. However, the same represent a burst of pulses which are synchronized to the beginning of data to be written and have a fixed length corresponding to the number of bits to be written. Thus under the circumstances here being described data clock pulses will correspond in number to 1700, the number of column bits written in each row.

The exemplary embodiment of a circuit suitable for separating data between odd and even columns illustrated in Figure 6 comprises first and second flip flops 70 and 72, a plurality of inverters 74 and 78, NAND gates 80 and 82 and an OR gate 84 whose inputs are inverted. The flip flops 70 and 72 may take the form of conventional D type flip flops which act in the conventional manner to present the logic condition applied at the D input thereto to its Q output whenever a clock pulse is applied during the presence of such D input. The complementary condition is maintained at the Q Not output. The clear input to each of the flip flops 70 and 72 is connected as indicated through conductors 86 and 88 to a system reset. The D input of each of the flip flops 70 and 72 is connected through conductors 90 and 92 to the Q Not or complementary output present at that flip flop. In similar manner, the Q output of each of the flip flops 70 and 72 is connected through conductors 94 and 96, respectively, to one input of a NAND gate 80 or 82 associated therewith. Thus, the exemplary clock pulse separation circuit illustrated in Figure 6 is highly symmetrical.

The clock input to the flip flop 70 is connected through a conductor 98 to an input annotated DACLK bar or the Data Clock Not input which represents the inverted data clock. The data clock, as was briefly noted above corresponds to the system clock in frequency, pulsewidth and polarity; however, the number of pulses present therein is limited to the number of bits to be written into the column drivers or in the case being discussed 1700. The data clock may be conveniently developed by ANDing the system clock with the output of a counter. This data clock is then inverted through the use of a conventional inverter in order that negatively directed clock pulses appropriate for switching the D flip flops 70 and 72 are obtained. The data clock input on conductor 98 is also supplied through conductor 100 to the inverters 74. The inverter 74 may take the conventional form of an inverter device which acts to produce a complement of an input at the output thereof and is here employed to ensure appropriate timing. The inverter 74 produces a complementary clocking level at it's output. The output of inverter 74 is applied through the conductor 102 to a second input of the NAND gate 80.

The NAND gate 80 acts in the conventional manner to produce a low at the output thereof on conductor 104 when both of the inputs thereto are high. Thus, when the Data Clock Not input on conductor 98 is high and the output of the flip flop 70 on conductor 94 is high, the output of NAND gate 80 will go low on conductor 104; however, when either input to NAND gate 80 is low the output on conductor 104 will be high. The output of the NAND gate 80 on conductor 104 is directly applied through conductor 106 to the terminal annotated $clock_1$ which is a signal directly employed in Figure 5 as a aforesaid. Thus, a negative pulse will be produced on conductor 106 to correspond with the presence of the first, third, fifth . . . .1699th clock pulses within the data clock.

The output of NAND gate 80 as present on conductor 104 is also applied as indicated in Figure 6 to one input of the OR gate 84 whose inputs are inverted. The OR gate 84 acts in the conventional manner of this well known class of device to produce a high at the output thereof on conductor 108 only when one of the inputs thereto is low. The output of OR gate 84 as supplied on conductor 108 is employed to generate the clock input for the second flip flop 72 after the same is inverted by the inverter 78 in the manner plainly illustrated in Figure 6. It will be appreciated that each time the $clock_1$ output on conductor 106 goes high or terminates the output of OR gate 84 will go low and after inversion by the inverter 78 will effectively act as a clock input to the second flip flop 72. This means that the Q Not output of flip flop 72 as supplied to the D input thereof on conductor 92 is clocked into the Q2 output thereof on conductor 96 when the $Clock_1$ output goes high or terminates.

A second input to the OR gate 84 is supplied through conductor 110 from the output of the NAND gate 82 on conductor 112. This output of the NAND gate 82 it will be noted corresponds to the $Clock_2$ output of the circuit or the clock output which comprises even pulses 2, 4, 6 . . . 1700 as present within the data clock. The NAND gate 82 whose output on conductor 112 is employed to generate the $Clock_2$ signal acts in the well known manner to produce a low at the output thereof on conductor 112 whenever both inputs thereto are high.

The first input to NAND gate 82 is supplied, as aforesaid, through conductor 96 from the Q output of flip flop 72. The second input to NAND gate 82 is connected through conductor 114 from the system clock as indicated in Figure 6. Thus those of ordinary skill in the art will appreciate that while the Q2 output of flip flop 72 will go high at the termination of the Clock 1 input, this input on conductor 96 to NAND gate 82 is gated by the system clock applied on conductor 114. Hence, while conductor

96 is primed at the termination of the Clock 1 input, the output of NAND gate 82 will not go low until the next clock signal is produced by the system clock, which is synchronized with the data clock, on conductor 114. Thus, it is during this interval of the system clock which is an even pulse that the output on conductor 112 which generates $Clock_2$ will go low.

In describing the operation of the exemplary circuit for separating data between odd and even columns as shown in Figure 6, it will be assumed that both flip flops 70 and 72 have been reset by reset levels on conductors 86 and 88. Under these conditions, the Q Not output of each flip flop will be high while the Q output thereof is low. When the first inverted data clock pulse is applied to conductor 98 flip flop 70 will clock the Q Not output which is high into the D input thereof and produce a high level on conductor 94. At the same time and for the duration of this first clock pulse the output of inverter 74 will be high producing the second high on conductor 102 and causing the output of NAND gate 80 to go low on conductor 104 for the duration of the first clock pulse. However, as soon as the first clock pulse terminates the output of inverter 74 will go low causing the output of NAND gate 80 to go high.

Thus, in this manner the first clock pulse corresponding in duration to the inverted data clock on conductor 98 is produced on conductor 106 as the Clock 1 signal. This same clock pulse on conductor 104 will cause the output of OR gate 84 to go high. This in turn will produce a low level or clocking input at the output of inverter 78 which is applied to the clock input of the second flip flop 72. This clock pulse will cause the Q Not output of flip flop 72 to be clocked into the D input thereof causing the Q2 output on conductor 96 to go high.

The high output on conductor 96, however, will not cause the output of gate 82 to go low until the occurrence of the second clock pulse which is received on conductor 114 from the system clock. Hence during the presence of the second clock pulse the output of NAND gate 82 will go low producing a negative going clock pulse on conductor 110 which corresponds to the $Clock_2$ signal. This $Clock_2$ pulse will stay low only for the duration of the second clock pulse received on conductor 114 from the system clock. Thus the $Clock_2$ output will go low and stay low for the duration of the second pulse in the system clock signal. This second clock pulse is also supplied through conductor 110 to OR gate 84 which acts to reset flip flop 72. Flip flop 70 is reset in a corresponding manner. Thus, it is seen that the circuit illustrated in Figure 6 will supply odd numbered clock pulses within the data clock at it's $Clock_1$ output while even numbered clock pulses present in the data clock are applied to the $Clock_2$ output thereof. Each clock signal present at the $Clock_1$ and $Clock_2$ outputs thereof are negative going clock pulses which correspond in duration to the clock pulse present in the data clock and system clock.

Referring now to Figures 7A-7C exemplary diagrams are set forth to illustrate the result of misalignment of connections between the contact pads of the frame illustrated in Figure 2 as illustrated by contact pads present in rows 34 and 36 as well as columns 38 and 40 and the contact pads 6 and 12 on the display. In this regard it should be noted that only highly simplified illustrations are set forth. Misalignments which generally occur would tend to be somewhat more complex.

Figure 7A shows an illustrative diagram of a portion of a display under conditions of proper alignment of the contact pads on the electrophoretic display panel apparatus shown in Figure 1 with the contact pads on the frame shown in Figure 2. More particularly, as shown in Figure 7A, it is assumed that an X is being displayed on a portion of the display panel illustrated in Figure 1 controlled by data supplied to column conductors 1-12 and row conductors 1-12. It will be appreciated that the X will be properly displayed when the rows and columns are connected in the manner illustrated in Figure 7A. It should be noted that proper column connection is assumed in all the illustrative examples set forth in Figures 7A-7C, however, corresponding misconnection thereof to that being discussed herein will result in corresponding misalignment problems where rows are improperly connected and under conditions where both columns and rows are misaligned, image rotation will additionally occur.

At any rate when each of the pads present in columns 38 and 40 are properly connected to their corresponding contact pads in the manner illustrated in Figure 7A, a properly configured X will be displayed on the panel in the manner illustrated in Figure 7A. Note in Figure 7A the proper alignment of the contact pads is shown by the opposite positioning of correspondingly numbered pads so that pad 1 is shown opposite pad 1, pad 2 is shown opposite pad 2, and at the bottom of each column pad 11 is shown opposite pad 11, while pad 12 is shown opposite pad 12. Under these conditions an X is properly designated and displayed it being noted that the coordinates for the driver lines associated with each element in the display for the X are shown in the elements of the X depicted in Figure 7A.

Figure 7B treats a case of simple misalignment in that while all of the row pads in the odd columns disposed along the left hand portion of the figure are properly aligned, a simple misalignment of one row has occured along the right hand set of pads

so that as illustrated in Figure 7B frame pad for row 4 is connected to display pad for row 2 and such misalignment by one row is continued. Under these conditions it will be seen that the X which should have been displayed is highly distorted for the simple misalignment condition being considered. In this regard it should be appreciated that in the actual assembling of such displays technicians may readily get correct alignment within an order of 4, however, perfect alignment is much more difficult to obtain and it is not at all infrequent that much time is spent in repositioning the frame structure. Obviously, misalignment by an order of 4 in Figure 7B would result in a much greater case of distortion and of course might well result in misalignment of the columns as well. This of course would produce a rotation of the distorted image.

It has been found according to one aspect of the instant invention that misalignment after the assembly of the display within the frame may be simply corrected through electronic means. This is accomplished by effecting a delay in the information applied to the non-misaligned pads which delay corresponds the number of clock pulses associated with the degree of misalignment. Accordingly when correction in this manner is implemented, as shown in Figure 7C, although some loss of information occurs the distorted information being displayed is corrected. Thus, it will be recalled in Figure 7B misalignment of one column had occured resulting in the distorted image of an X shown in Figure 7B. If however the information provided to the rows which are not misaligned, i.e. those illustrated at the left-hand portion of Figure 7C, is delayed by the number of clock pulses corresponding to the misalignment, the image depicted is corrected even though some information is lost. Thus, in Figure 7C it will be seen that the row pads associated with the right-hand side of the figure are misaligned by one row. Therefore, referring to the left-hand side of the illustration the information provided to the properly aligned row pads is delayed by one clock cycle so that information for row 3 is provided to row 1. Thus a delay corresponding to one clock cycle is provided to all row information for the odd rows illustrated along the left-hand portion of Figure 7C. The X now displayed in Figure 7C is correct and looks like an X except that the two top lines of information have been lost. This distortion is extremely slight compared to what is produced in Figure 7B.

Referring now to Figure 8, there is shown an illustrative block diagram of an exemplary alignment correction circuit in accordance with the teachings of the instant invention and more particularly an exemplary circuit for implementing the correction illustrated in Figure 7C or the like. The circuit illustrated in Figure 8 is connected for example in series with the data input supplied to the circuit shown in Figure 5 for the odd column connectors and receives its input from the data stream normally applied to the Data In input on conductor 50 as illustrated in Figure 5. It is envisioned that one circuit of the type illustrated in Figure 8 shall be applied to each of the odd and even column driver circuits employed with the electrophoretic display panel apparatus according to the instant invention and conversely a circuit of the type illustrated in Figure 8 shall also be applied to each of the odd and even row driver circuits employed. In the case of the row driver circuits, only the clock rate defines the row to be energized but the same may be treated in similar manner to data. The exemplary embodiment of the circuit illustrated in Figure 4 is capable of correcting misalignment problems of the type described in association with Figure 7A-7C for up to eight levels of misalignment of the pads associated with an odd or even row or column. The circuit of Figure 8 is basically a delay device and hence if the odd rows were misaligned correction would be implemented on the even rows and vise versa and the same situation obtains for the columns.

The illustrative block diagram of the alignment correction circuit illustrated in Figure 8 comprises eight switches indicated generally by switches D_0-D_7, eight gating circuits 119-126 and eight flip flops 130-137. In brief, the circuit is operative to insert one clock cycle of delay into a signal for each switch D_0-D_7 that is opened while if the switch is left in a closed position no delay is inserted. The switches must be opened in numerical order and the circuit receives data on the right and outputs data at the left.

The exemplary circuit as illustrated in Figure 8 is symmetrical and constructed in stages, each stage corresponding to one element of delay. More particularly, each of the switches D_0-D_7 is a single throw switch which connects between ground as shown in its closed position and a junction connected to 5 volts DC through a resistor R1, an input to an associated inverter I_0-I_7 and one input to an associated one of gate chips 119-126.

Each of the gate chips 119-126 may comprise a conventional 7451 chip as available from Texas Instrument Corporation or the like. Each of the gate chips 119-126 has been illustrated as comprising a pair of AND gates A_1 and A_2 and a NOR gate $_{N1}$. Each of the AND gates A_1 and A_2 act in the conventional manner of this well-known class of device to produce a high output only when both of the inputs thereto are high while producing a low when any input thereto is low. The NOR gates N_1 comprise conventional forms of this well-known class of device and act to produce a low at the output thereof when either of the inputs thereto are

high. The inputs to each of the NOR gates N_1 are provided from the outputs of the AND gates A_1 and A_2 within each of gate chips 119-126. Furthermore, each of gate chips 119-126 are provided with inputs in a corresponding manner. The outputs of each gate chip 119-126 as taken from the output of the NOR gate N_1, is inverted through one of inverters 140-147 and provided to either the data output of this circuit in the case of inverter 140 or to the flip flop 130-136 associated with the output of that stage.

Each of the flip flops 130-137 are conventional D-type flip flops which act in the manner described in connection with Figure 6 to assume the level applied to its D input in the presence of a clock pulse. The D inputs to each of the flip flops 130-136 are connected to the inverter 141-147 associated with that stage while the D input to flip flop 137 receives the data input to the circuit as indicated by the terminal 150. The Clock input to each of the flip flops 130-137 is supplied with a Clock 1 or Clock 2 input provided to the odd or even row or columns to which it is assigned. This clock input is developed in the precise manner as was described in connection with Figure 6. The clock input as indicated in Figure 8 is inverted by a pair of conventional inverters 154 and 156 and thereafter applied to the clock input of each of the flip flops 131-136 through the conductor 158. The Data In input which, in the case of column drivers, would correspond to the Data In input on conductor 52 in Figure 5 is applied through a pair of inverters 160 and 162 to the D input of the flip flop 137 and one of the inputs to the A_1 AND gate present in each of the gate circuits 119-126.

In operation it is contemplated that one circuit such as illustrated in Figure 8 will be provided for each of the odd and even column driver circuits as well as each of the odd and even row driver circuits. After assembly of the display into the frame illustrated in Figure 2 all the switches D_0-D_7 in each of the four delay arrays provided will be closed. Thereafter the display will be energized and the operator will note any misalignment problems on the screen. For instance, if a result such as illustrated in Figure 7B occurred, it would be clear that misalignment has occurred with respect to one of the rows present in the even side of the panel. This would require that one switch D_0 be closed in the delay array illustrated in Figure 8 assigned to the odd side of the panel so that the correction illustrated in Figure 7C can be obtained. Under these circumstances switch D_0 would be opened while all the remaining switches remain closed.

From an inspection of Figure 8 those of ordinary skill in the art will appreciate that when D_0 is closed, the inputs associated with AND gate A_1 in each of the gate arrays 119-126 is enabled while when the switch is opened to insert delay, AND gate A_1 is disabled while AND gate A_2 is enabled. This means that the bit of data being processed will be processed through the preceding gate array and its output, delayed by one clock pulse in the flip flop associated therewith and gated through the A_2 AND gate within the next gate array in the following clock cycle.

For instance, if it is assumed that perfect alignment has been achieved all the switches D0-D_7 would be closed. Under these circumstances the output of inverter I_0 would be high predisposing AND gate A_1 in the gate array 119 to follow the condition of data applied to terminal 150 and subsequently through the inverters 160 and 162 to the other input of the AND gate A_1. If this data bit were high this would result in a high, at the output of AND gate A1 within the gate array 119. Since under these conditions switch D_0 is closed, one input to AND gate A_2 will be low so that this gate is effectively disabled. When the output of AND gate A_1 goes high, the output of NOR gate N_1 will go low. This low will be inverted by the inverter 140 and an appropriate, undelayed data bit, will be supplied to the driver circuit illustrated in Figure 5.

However, if it is assumed that one element of delay is to be inserted, switches D_1-D_7 would remain closed while switch D_0 would be opened. Under these conditions a high level would be present at one input to AND gate A_2 while a low is imposed on the input of AND gate A_1 connected to the inverter I_0. Hence AND gate A_1 is effectively disabled. Under these conditions gate array 120 would be effectively enabled for the receipt of the first bit of data. Therefore, when this bit of data is applied to AND gate A_1 which is enabled by a high from the output of inverter I_1, the output of AND gate A_1 in gate array 120 would go high placing a high at the input to NOR gate N_1. Thus if the first data bit on input terminal 150 were high, the output of AND gate A_1 within the gate array 120 would go high causing the output of NOR gate N_1 to go low. This would be inverted by the inverter 141 and would cause the Q-output of the flip flop 130 to go high when the next clock pulse was applied to conductor 158. Thus, the data bit would be loaded into the flip flop 130 with the next clock pulse and applied to the second input of AND gate A_2 within the gate array 119. Once this occurs, the output of A_2 due to the open condition of switch D_0 would go high causing a low to be gated out of NOR gate N_1 and a high to be supplied to the data output connected to the output of the inverter 140.

Those of ordinary skill in the art will appreciate that in precisely the foregoing manner one element of delay is inserted for each of the switches D_0-D_7 that is opened and hence correction of the type

illustrated in Figure 7C may be readily implemented with the arrangement set forth in Figure 8. Once correction has been implemented by a technician, the switches D_5-D_7 are fixed and in certain embodiments it may be desired to burn the switches into their set positions so that they may not be altered. Alternatively, merely placing the switches at inexcessible locations may suffice and this is viewed as highly advantageous since the same will facilitate readjustment in a case where changing of the display in the field may be desired.

Those of ordinary skill in the art will appreciate that the instant invention admits of many adaptations and variations to suit choice of design. For instance, more or less delay stages of the type shown in Figure 8 may be provided and the same may be implemented using different techniques. Further, in connection with the tined grid structure illustrated in Figures 3 and 4 it will be appreciated that a greater or fewer number of tines may be employed for purposes of maximizing contrast or providing specialized forms of contrast suited to a particular application. In this regard, it may additionally be noted that depending upon the types of colors employed in the electrophoretic display panel apparatus, contrast will vary and for this reason too either a greater or lesser number of tines may be desired.

Those of ordinary skill in the art will readily appreciate the instant invention provides techniques whereby electrophoretic displays may be properly aligned and maximized with respect to contrast while manufacturing and assembling thereof at modest cost may be realized. Thus, while rather specific manufacturing details of the electrophoretic display contemplated herein have been set forth, the instant invention will have wide application to any form of manufacturing and assembling of these types of displays and are not limited to the specific manner of mating frame with display as described herein.

It will be appreciated, therefore, that one aspect of the present invention provides an electrode panel of an electrophoretic display having a first plurality of conductors extending transversely to, insulated from and forming crossing points with a second plurality of conductors, each of at least one of said pluralities of conductors comprising a plurality of parallel, commonly connected conductor portions. Another aspect of the present invention provides an electrophoretic display having a first plurality of conductors crossing a second plurality of conductors and a multiplex driving means including means to introduce a delay into drive signals applied to some of the conductors in at least one of the pluralities of conductors.

Claims

1. Electrophoretic display panel apparatus comprising;
a planar member;
a first plurality of conductive lines deposited in a first direction on said planar member, each of said first plurality of conductive lines being disposed in parallel on said planar member; a second plurality of conductive lines disposed in a second direction on said planar member, said second direction being transverse to said first direction, each of said second plurality of conductive lines spacially crossing each of said first plurality of conductive lines to form a plurality of intersections therebetween and each of said second plurality of conductive lines including a plurality of commonly connected, parallel line segments extending in said second direction to form a plurality of minor intersections with each of said firt plurality of conductive lines at each of said plurality of intersections;
means for insulating each of said plurality of commonly connected, parallel line segments in each of said second plurality of conductive lines from each of said first plurality of conductive lines; and
means overlying said planar member and said first and second plurality of conductive lines for establishing a fluid tight panel, said means overlying creating a space above said planar member and said first and second plurality of conductive lines for maintaining an electrophoretic dispersion.

2. An apparatus according to Claim 1 wherein said means for insulating underlies said parallel line segments in each of said second plurality of conductive lines and establishes troughs intermediate adjacent parallel line segments, said troughs acting as wells from which and to which electrophoretic particles may displace.

3. An apparatus according to Claim 1 or 2 additionally comprising means for applying potential to each conductive line within said first and second pluralities of conductive lines.

4. An apparatus according to any preceding claim additionally comprising contact pad means formed at an end portion of each conductive line within said first and second pluralities of conductive lines.

5. An apparatus according to Claim 4 wherein said panel member is rectangular and exhibits first, second, third and fourth side portions and said contact pad means formed at end portions of each conductive line within said first plurality of conductive lines are exposed from and proximate to said first and second side portions and said contact pad means formed at end portions of each conductive line within said second plurality of conductive lines are exposed from and proximate to said third and fourth side portions.

6. An apparatus according to Claim 5 wherein said first and second pluralities of conductive lines each contain odd and even number conductive lines and said contact pad means formed at said end portions of each odd number conductive line within said first plurality of conductive lines is exposed from and proximate to said first side portion; said contact pad means formed at said end portions of each even number conductive line within said first plurality of conductive lines is exposed from and proximate to said second side portion, said contact pad means formed at said end portions of each odd number conductive line within said second plurality of conductive lines is exposed from and proximate to said third side portion and said contact pad means formed at said end portions of each even number conductive line within said second plurality of conductive lines is exposed from and proximate to said fourth side portion.

7. An apparatus according any of Claims 4 to 6 additionally comprising means for selectively applying potential to each conductive line within said first and second pluralities of conductive lines, said means for selectively applying including means for establishing electrical contact to each of said contact pad means and means for selectively delaying potential applied to predetermined ones of said contact pad means to compensate for misalignment in established electrical contact to each of said contact means.

8. An apparatus according to Claim 7 wherein said contact pad means for each conductive line within said first plurality of conductive lines are disposed in a pair of columns and said contact pad means for each conductive line within said second plurality of conductive lines are disposed in a pair of rows, said contact pad means within each pair of rows and columns being grouped according to an odd and even designation.

9. An apparatus according to Claim 8 wherein said means for selectively delaying potential applied to predetermined ones of said contact pad means is independently operative in respect to each column and row within said pairs of columns and rows.

10. An apparatus according to Claim 8 or 9 wherein said means for selectively applying potential acts when enabled to selectively apply potential in the for of One's and Zero's to each contact pad means in one row of said pair and a potential level to one contact pad means in said pair of columns.

11. Electrophoretic display panel apparatus comprising

a first plurality of conductive lines deposited in parallel on a planar member;

a second plurality of conductive lines disposed in parallel on said planar member in a direction transverse to said first plurality of conductive lines, said second plurality of conductive lines being insulated from said plurality if conductive lines;

means overlying said planar member and said first and second plurality of conductive lines for establishing a fluid tight panel, said means overlying creating a space above said planar member and said first and second plurality of conductive lines for maintaining an electrophoretic dispersion; and

means for selectively applying write signals to said first and second plurality of conductive lines, said means for selectively applying including means for connecting said write signals to each of said first and second plurality of conductive lines, and means for selectively delaying write signals selectively applied to predetermined ones of said first and second plurality of conductive lines to compensate for misalignment in said means for connecting.

12. An apparatus according to Claim 11 wherein said means for selectively applying write signals acts to selectively apply write signals to selected ones of said first and second plurality of conductive lines at a predetermined clocking rate and said means for selectively delaying acts to selectively delay said write signals applied to predetermined ones of said first and second plurality of conductive lines by a selectable number of delay intervals defined by said clocking rate.

13. An apparatus according to Claim 12 wherein said means for selectively delaying includes a plurality of serial connected delay stages, each of said plurality of serial connected delay stages being configured to insert one delay interval in write signals selectively applied to said predetermined ones of said first and second plurality of conductive lines.

14. An apparatus according to Claim 13 wherein each of said delay stages includes switch means for selectively enabling the delay stage associated therewith to cause said delay interval to be inserted in write signals selectively applied to said predetermined ones of said first and second plurality of conductive lines.

15. An apparatus according to Claim 11 wherein said first and second plurality of conductive lines are each separately designated as odd and even conductive lines within said first and second plurality of conductive lines and said means for selectively applying write signals acts to selectively apply write signals alternatively to odd and even conductive lines within said second plurality of conductive lines.

16. An apparatus according to Claim 15 wherein said means for selectively delaying write signals includes at least a first delay circuit associated with said odd conductive lines and a second delay circuit associated with said even conductive lines.

17. An apparatus according to Claim 16 wherein said first delay circuit is activated if misalignment occurs with respect to said even conductive lines and said second delay circuit is activated if misalignment occurs with respect to said odd conductive lines.

18. An apparatus according to any of Claims 15 to 17 wherein said means for selectively applying write signals acts to selectively apply write signals to said odd and even conductive lines at a predetermined clocking rate and said means for selectively delaying acts to selectively delay said write signals selectively applied to said odd and even conductive lines by a selectable number of delay intervals defined by said clocking rate.

19. An apparatus according to Claim 18 wherein said means for selectively delaying write signals includes at least a first delay circuit associated with said odd conductive lines and a second delay circuit associated with said even conductive lines.

20. An apparatus according to Claim 19 wherein each of said first and second delay circuits includes a plurality of serial connected delay stages, each of said plurality of serial connected delay stages being configured to insert one delay interval in write signals selectively applied to said conductive lines.

21. An apparatus according to Claim 20 wherein said first delay circuit is activated if misalignment occurs with respect to said even conductive lines and said second delay circuit is activated if misalignment occurs with respect to said odd conductive lines.

22. An apparatus according to any of Claims 11 to 21 wherein each of said second plurality of conductive lines spacially cross each of said first plurality of conductive lines to form a plurality of intersections therebetween and each of said second plurality of conductive lines include a plurality of commonly connected, parallel line segments extending in said second direction to form a plurality of minor intersections with each of said first plurality of conductive lines at each of said plurality of intersections.

23. An apparatus according to Claim 22 wherein said second plurality of conductive lines are insulated from said first plurality of conductive lines by means for insulating, said means for insulating underlying said parallel line segments in each of said second plurality of conductive lines and establishing troughs intermediate adjacent parallel line segments, said troughs acting as wells from which and to which electrophoretic particles may displace.

24. An apparatus according to any of Claims 11 to 23, additionally comprising contact pad means formed at an end portion of each conductive line within said first and second pluralities of conductive lines.

25. An apparatus according to Claim 2 or 23, or any claim dependent on Claim 2 or 23 wherein said troughs are additionally established intermediate adjacent ones of said second plurality of conductive lines.

26. An apparatus according to any preceding claim wherein said planar member and said first plurality of conductive lines are substantially transparent.

27. An apparatus according to any preceding claim wherein said means overlying is substantially transparent.

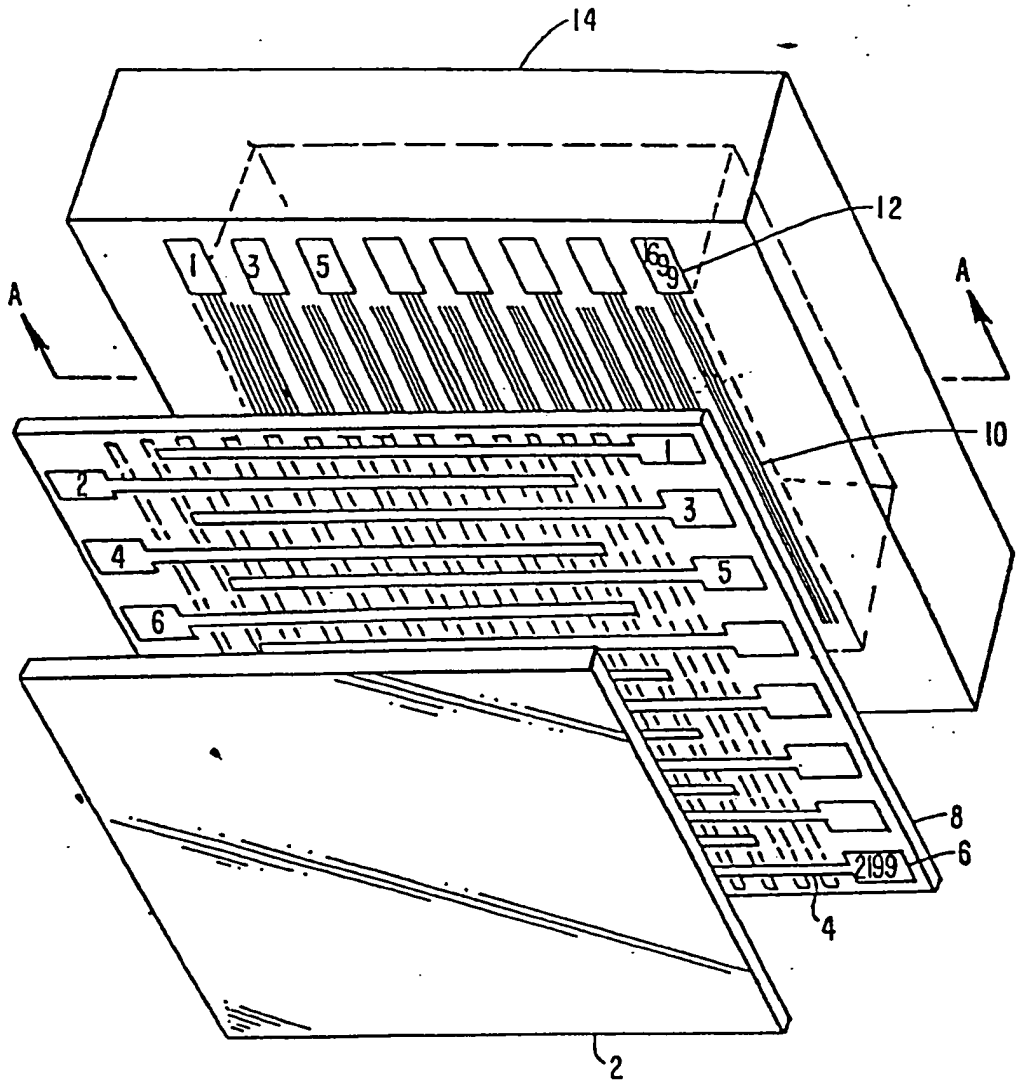

FIG. 1

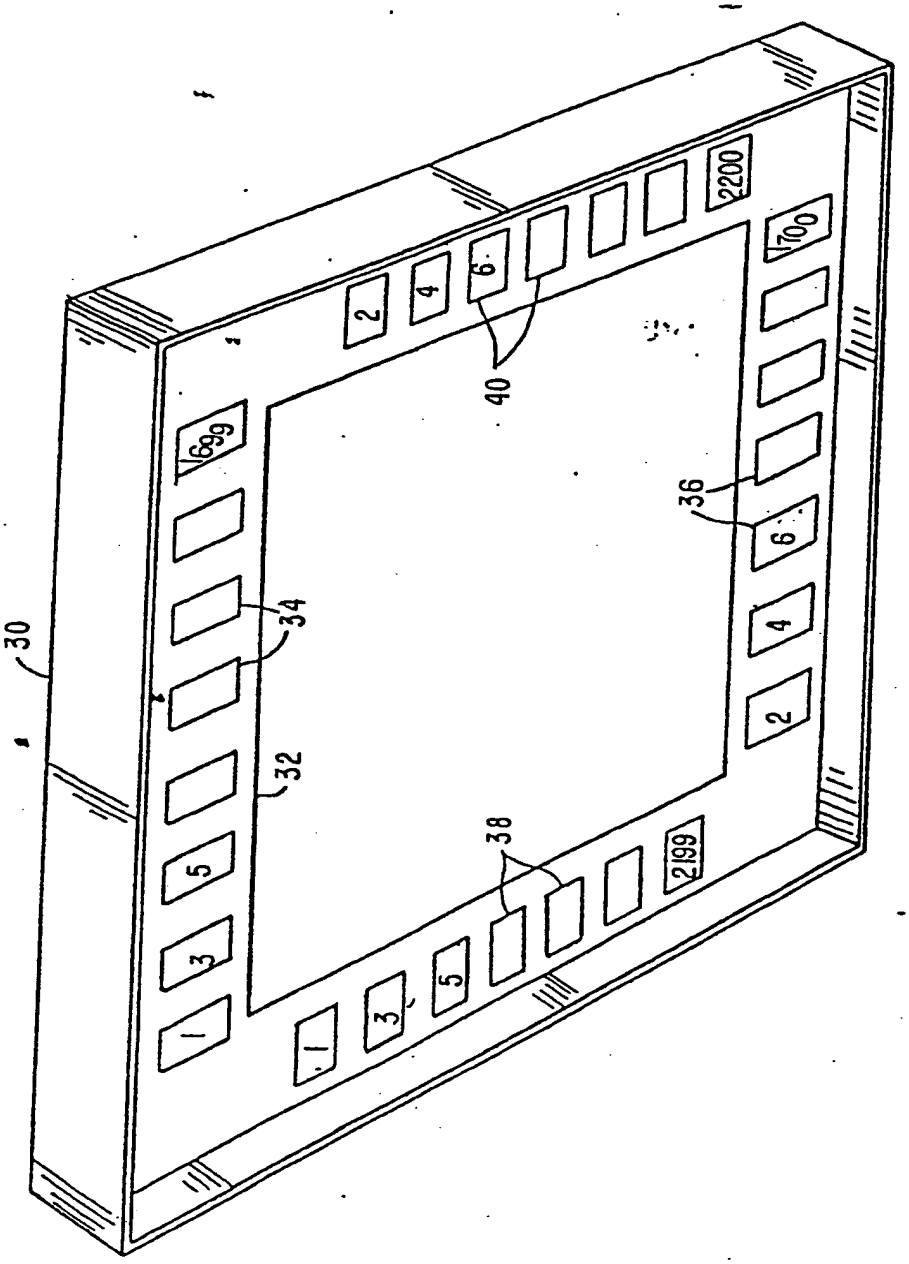

FIG. 2

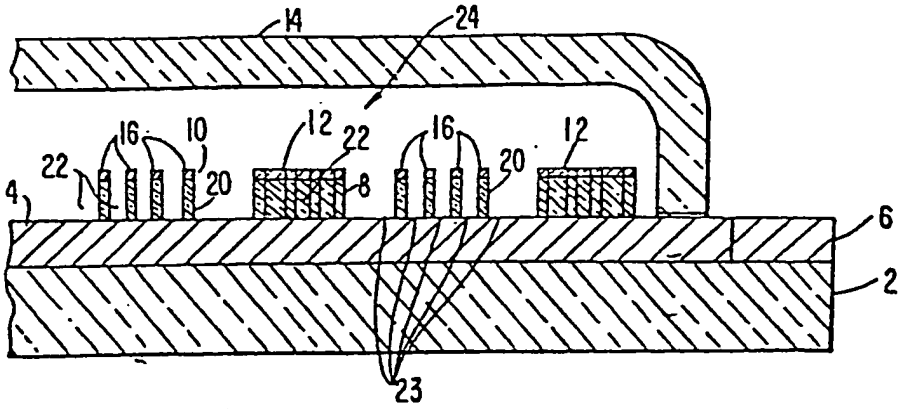

FIG. 3

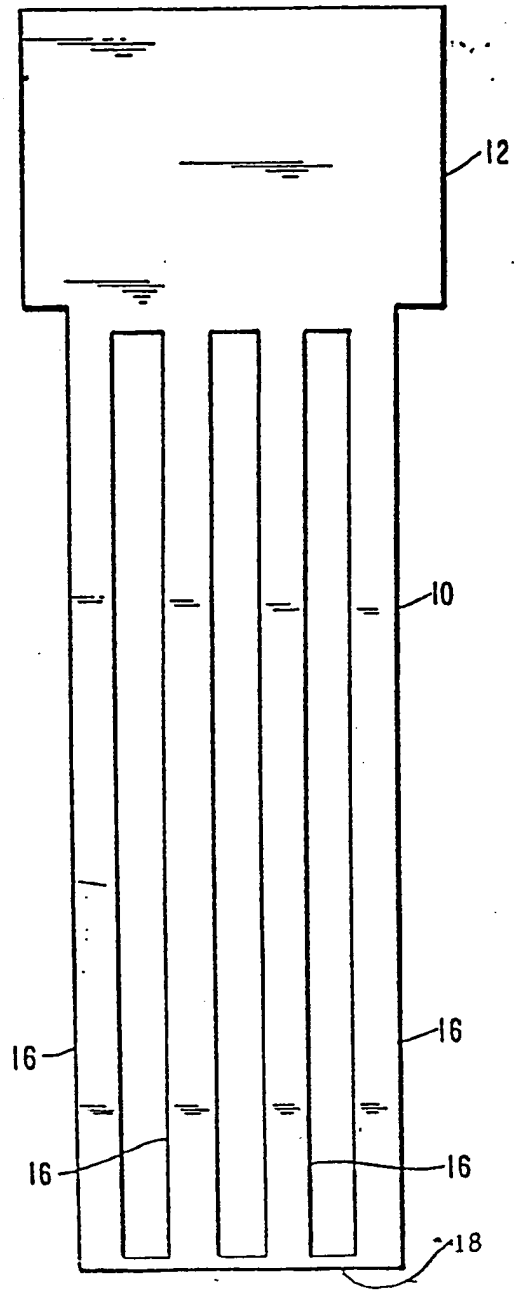

FIG. 4

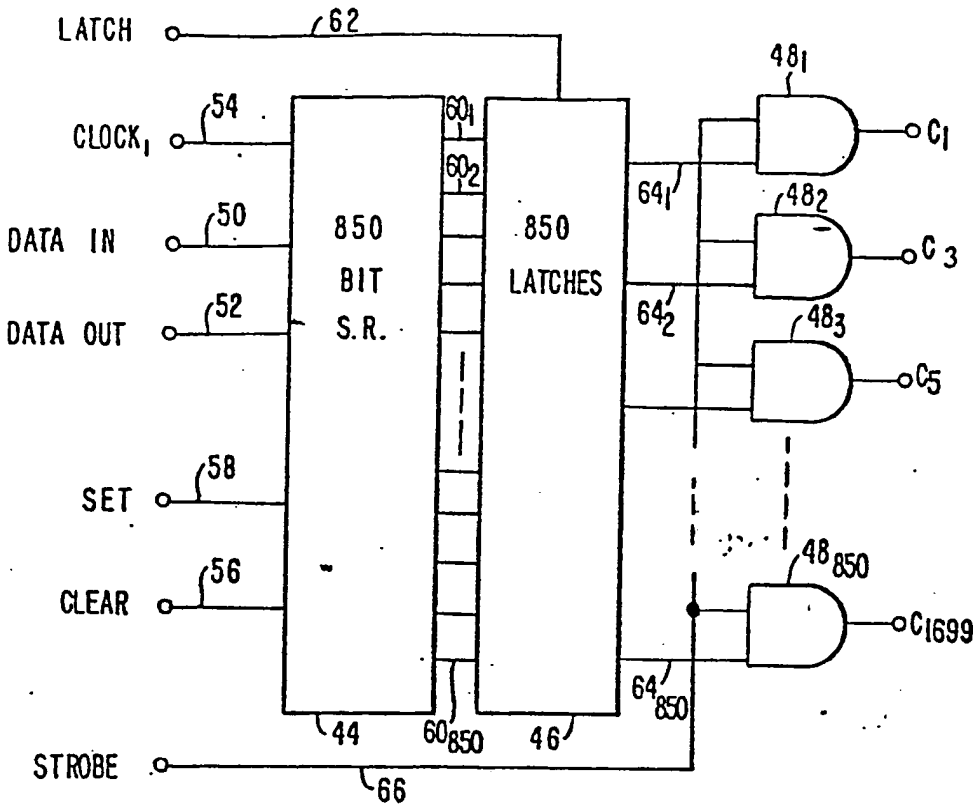
LATCH
62
CLOCK1
54
DATA IN
50
DATA OUT
52
SET
58
CLEAR
56
STROBE
66
850 BIT S.R.
850 LATCHES
44
46
60850
64850
481
482
483
48850
C1
C3
C5
C1699

FIG. 5

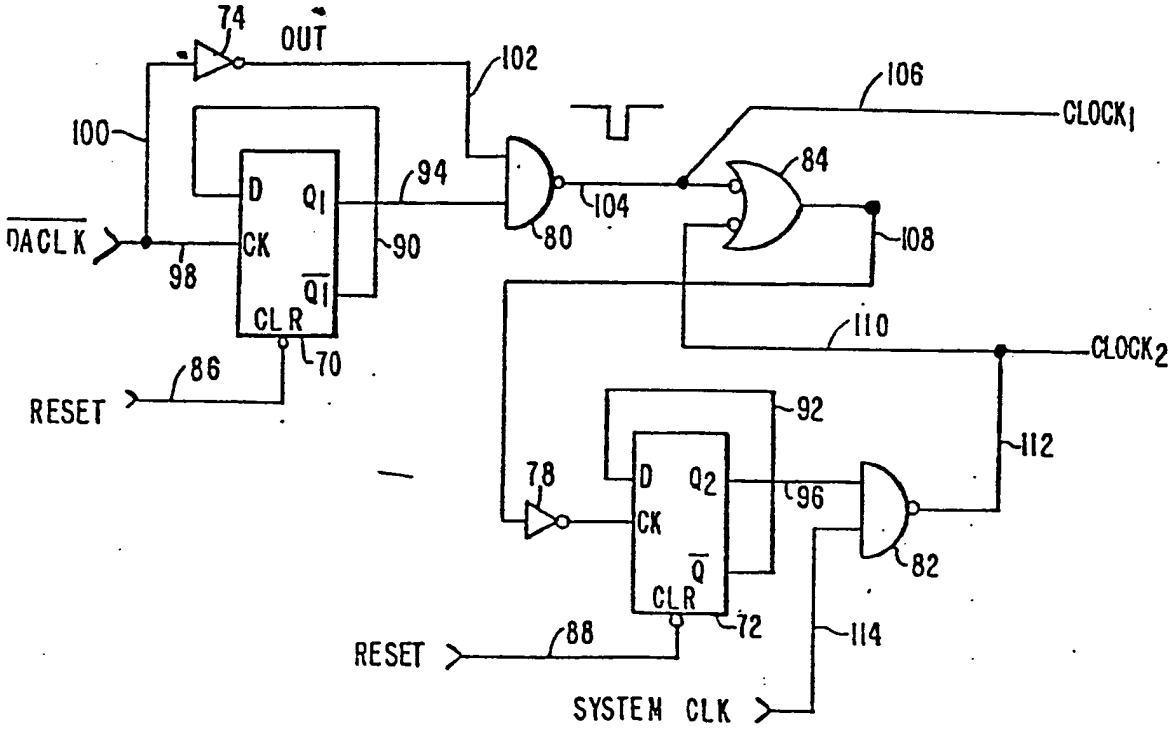
74
OUT
102
106
CLOCK1
100
94
84
104
80
108
DACLK
98
90
CK
CLR
86
RESET
70
110
CLOCK2
92
112
78
96
82
88
72
114
SYSTEM CLK

FIG. 6

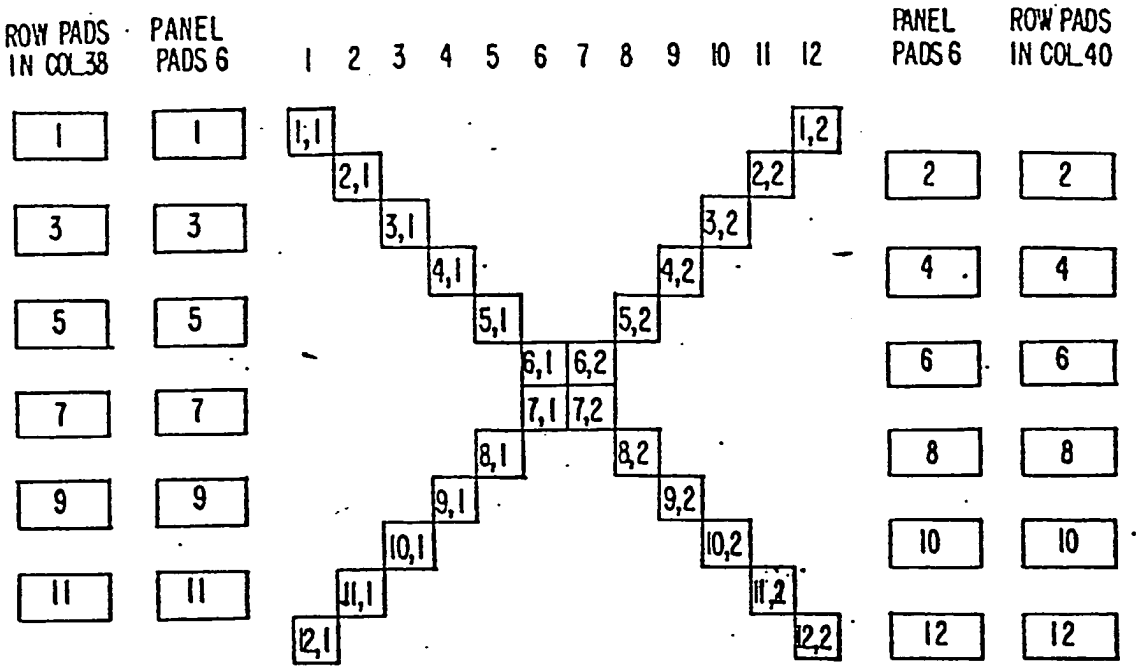
ROW PADS IN COL 38
PANEL PADS 6
1 2 3 4 5 6 7 8 9 10 11 12
PANEL PADS 6
ROW PADS IN COL 40
1
3
5
7
9
11
1,1
2,1
3,1
4,1
5,1
6,1
7,1
8,1
9,1
10,1
11,1
12,1
1,2
2,2
3,2
4,2
5,2
6,2
7,2
8,2
9,2
10,2
11,2
12,2
2
4
6
8
10
12

FIG. 7A

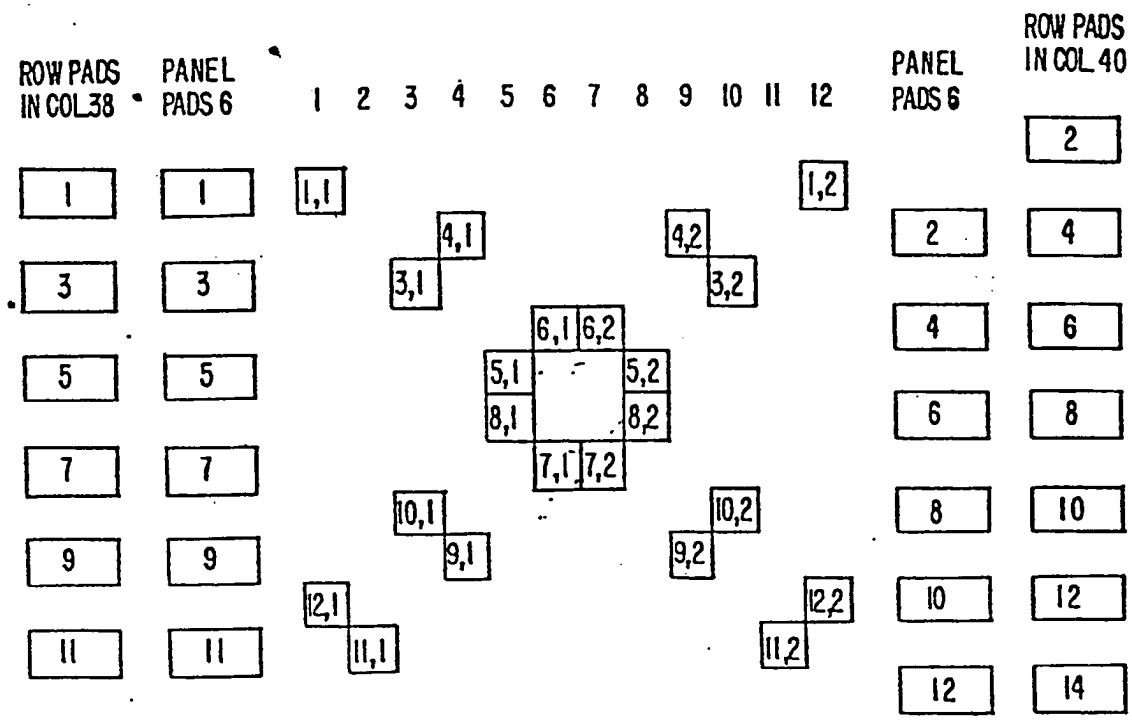
ROW PADS IN COL 38
PANEL PADS 6
1 2 3 4 5 6 7 8 9 10 11 12
PANEL PADS 6
ROW PADS IN COL 40
1
3
5
7
9
11
1,1
4,1
3,1
6,1
6,2
5,1
5,2
8,1
8,2
7,1
7,2
10,1
9,1
10,2
9,2
12,1
11,1
1,2
12,2
11,2
2
4
6
8
10
12
2
4
6
8
10
12
14

FIG. 7B

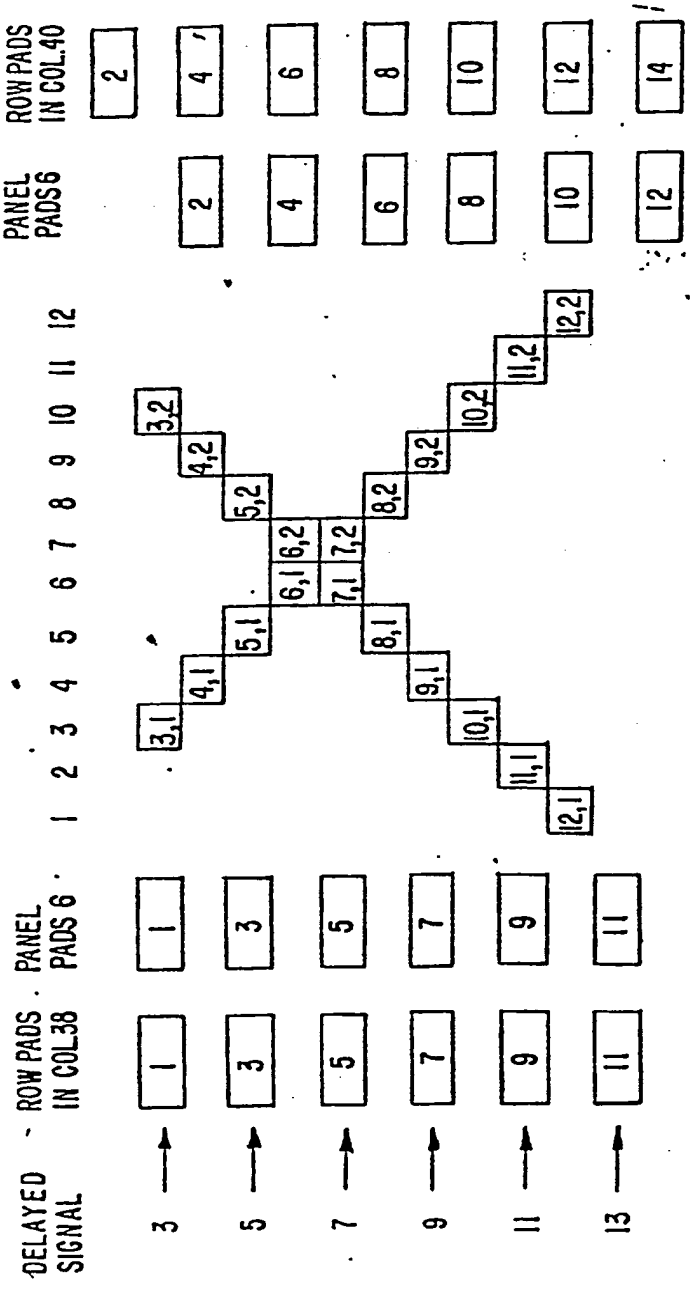
DELAYED SIGNAL
ROW PADS IN COL.38
PANEL PADS 6
1 2 3 4 5 6 7 8 9 10 11 12
PANEL PADS6
ROW PADS IN COL.40
3,1
4,1
5,1
6,1
6,2
5,2
4,2
3,2
7,1
7,2
8,1
8,2
9,1
9,2
10,1
10,2
11,1
11,2
12,1
12,2

FIG. 7C

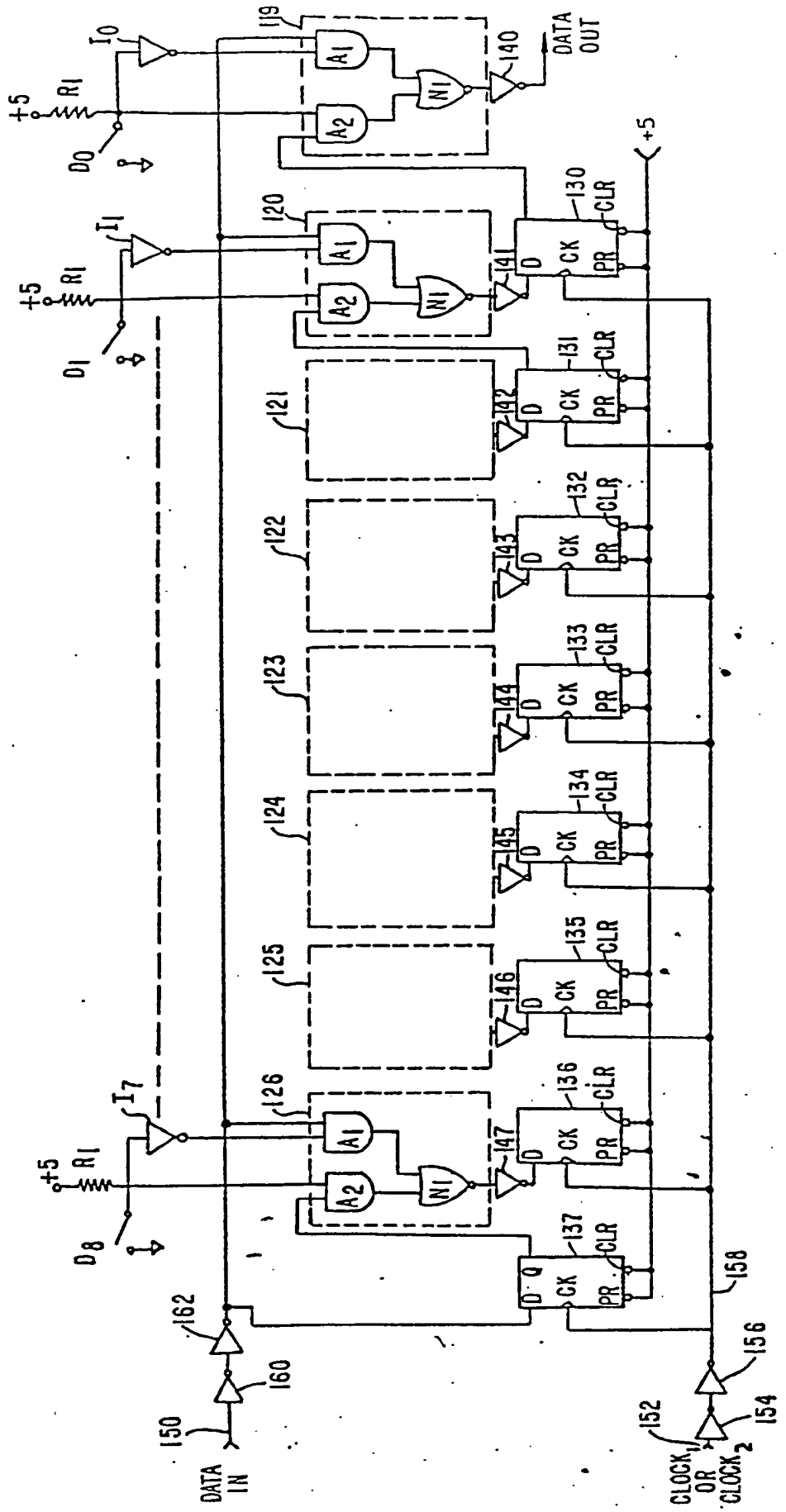
DATA OUT
DATA IN
CLOCK1 OR CLOCK2
+5
R1
I0
I1
I7
D0
D1
D8
A1
A2
N1
CK
PR
CLR
D
Q

FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 30 0448

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	CONFERENCE RECORD OF 1980 BIENNIAL DISPLAY RESEARCH CONFERENCE, 21st-23rd October 1980, Cherry Hill, N.J., pages 26-30, IEEE, New York, US; R. LIEBERT et al.: "A 512 character electrophoretic display" * Page 27, column 2, lines 4-19; page 30, column 1, lines 35-41; figure 2 *	1-5	G 02 F 1/19 G 09 G 3/34
A	IDEM	11	
A	EP-A-0 187 054 (THOMSON-CSF) * Page 5, lines 10-18; figure 3 *	6,8	
A	EP-A-0 145 143 (SHARP) * Page 7, lines 3-20; page 9, line 12 - page 11, line 24; figures 1,2 *	7,9,11	
A	EP-A-0 097 799 (IBM) * Page 11, lines 17-31; figure 3 *	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4) G 02 F G 09 G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30-08-1988	LOFFREDO A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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